NOVEL INDUCTORLESS NEURISTOR LINE

Indexing terms: Delays, Neural nets

A novel inductorless neuristor line having the desired properties of the axon is described. Each section of the line consists of a pair of *p–n–p–n–p–n* transistors and an *RC* circuit with small capacitor values. This allows integration of the line using semiconductor technology.

There are great difficulties in the integration of known neuristor line models because of the necessity of using large capacitances of the order of several thousands of picofarads[1, 2, 7] or the necessity of inductances.[4, 5, 9] Moreover, most of the proposed models[2, 4, 6–8] do not exhibit all of the following desired properties of the axon:

(*a*) constant pulse-propagation velocity

(*b*) threshold point (if pulse height exceeds it, pulse propagation is possible, if not, the pulses are attenuated)

(*c*) the pulse-shaping action during its propagation through the line

(*d*) refractory period

(*e*) annihilation of pulses in the case of their collision.

The proposed neuristor line model is based on the lumped delay line of the 'thyristor–*RC*' type shown in Fig. 1*a*. In a steady state, transistors T_1 and T_2, which form a 'thyristor' subcircuit, are cutoff, since the capacitors C_1 and C_2 are charged up to the supply voltage V_b. Application of a negative pulse, with respect to V_b, to the input port turns the transistors T_1 and T_2 into their active regions of operation and then causes saturation of T_2. The saturation time for T_2, which determines the output pulsewidth, is determined by the discharge time of the capacitor C_1 through the resistance R_3 in parallel with the nonlinear input resistance of T_2 and the storage time of transistor T_2. The charging time of C_1 through resistance R_4, after the cutoff of T_1, assures the existence of a refractory period in the line. Delay of the transmitted pulse is achieved by the integrating circuits formed by R_1 and C_2, which are connected between active sections of the line.

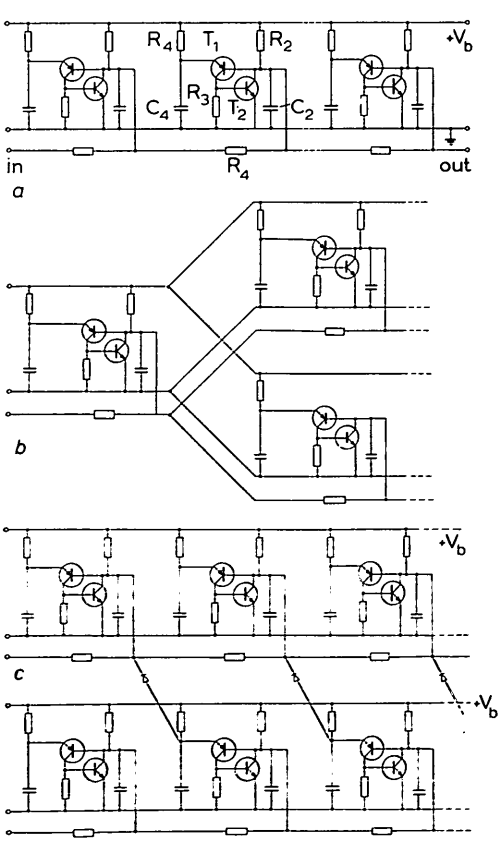

Fig. 1 *Proposed inductorless neuristor line*
a Schematic. $R_1 = 10\,k\Omega$, $R_2 = 5{\cdot}6\,k\Omega$, $R_3 \simeq 3\,k\Omega$, $R_4 = 30\,k\Omega$, $C_1 = C_2 = 50\,pF$
b Type-T junction realisation
c Type-R junction realisation

Constant pulse-propagation velocity: Constant pulse-propagation velocity in the line is caused by the delay time t_1 of the input pulse, which is applied through the integrating circuit $R_1 C_1$ to each active section of the line. The delay time t_1 is determined by the relationship

$$t_1 = -\frac{R_1 C_2}{a} \ln\left[1 - a\frac{V_{BE1}}{V_{in}}\right] \quad (1)$$

where V_{BE1} is the minimum base–emitter voltage on transistor T_1 which is necessary for saturation of T_2, V_{in} is the amplitude of the input pulse with respect to V_b and $a = R_1/R_2 + 2$.

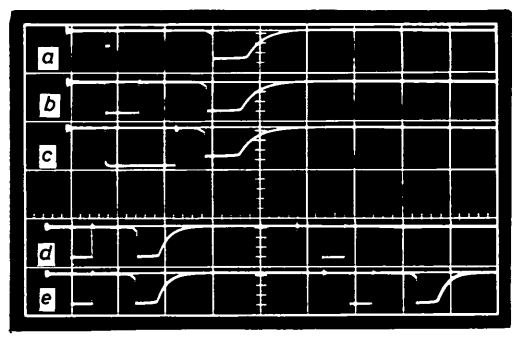

Fig. 2 *Experimental results*
The first pulse is an input pulse and the second pulse is an output one-on-four section
a, *b*, *c*: The pulse-shaping action. Horizontal scale is 0·3 μs/division, vertical scale is 15 V/division
d Pulse period smaller than the refractory time
e Pulse period greater than the refractory time
d and *e* Horizontal scale is 0·5 μs/division, vertical scale is 15V/division

Threshold point: To initiate the regeneration process in each active section it is necessary to apply a negative input pulse having the amplitude greater than V_p:

$$V_{in} \geqslant V_p = aV_{BE1} \quad (2)$$

The duration of the input pulse with this amplitude should be large enough to allow transistor T_1 to turn on into its active region, usually greater than t_1.

Pulse-shaping action: The shaping of the propagated pulse through the line depends on the time constant $R_{BE2} \| R_3/C_1$ and on the storage time τ of the transistor T_2. The propagated pulse duration time t_2,

$$t_2 = [R_{BE2} \| R_3]\, C_1 \ln\left[\frac{V_b}{V_{BE2}}\right] + \tau \quad . \quad . \quad . \quad . \quad (3)$$

is determined by the first component of eqn. 3, i.e. by the time after which the voltage between the base and emitter of T_2 becomes smaller than the voltage V_{BE2} determining the cutoff state of T_2. In a practically realised circuit, the storage time τ was negligible. The output pulse amplitude is approximately equal to the supply voltage V_b.

Refractory period: The refractory period of the line is caused by the existence of the cutoff base–emitter voltage at the transistor T_1 after passing of the pulse through each section of the line. The refractory time t_3 is expressed in terms of the charging time of C_1 and the propagated pulse-duration time t_2:

$$t_3 = R_4 C_1 \ln\left[\frac{V_b - V_{BE2}}{(V_{in}/a) - V_{BE1}}\right] + t_2 \quad . \quad . \quad . \quad . \quad (4)$$

Annihilation of pulses: Annihilation of pulses in the case of their collision when pulses are propagating from opposite directions is a consequence of the existence of the refractory period, which causes pulse attenuation. The practical importance of proposed neuristor line models depends on simple realisations of T-type and R-type junctions.[3] These are shown in Figs. 1*b* and *c*, respectively, for this line. These junctions

allow realisation of neuristor logic elements[3, 10] used for simulated neural networks. The experimental results for the discussed neuristor line are shown in Figs. 2*a–e*. The conclusion is that the proposed line model has all the desired properties of the axon necessary for simulation of complex neural networks. The capacitances used in the practical model for $t_1 = 0{\cdot}05$, $t_2 = 0{\cdot}025$ and $t_3 = 3\ \mu s$ are smaller than 50 pF. This allows for full integration using monolitic semiconductor technology. Additionally, the *p–n–p* transistor T_1 may have small current gain, allowing the use of lateral transistors in a practical integrated realisation. In the resting state of the line, when all transistors are cut off, no power is consumed from the supply battery.

Acknowledgment: The work was supported by the US National Science Foundation under Grant GF-42178.

B. M. WILAMOWSKI
Z. CZARNUL
M. BIALKO

Institute of Electron Technology
Technical University of Gdańsk
Majakowskiego 11/12, 80–952 Gdańsk, Poland

23rd June 1975

References

1 AMBROZIAK, A.: 'Semidistributed neuristor line using unijunction transistors', *Solid-State Electron.*, 1964, **7**, pp. 259–265
2 COTE, A. J.: 'Simulating nerve networks', *Electronics*, 1961, **34**, pp. 51–53 and 'Neuristor propagation in long tunnel diodes', *Proc. Inst. Elec. Electron. Eng.*, 1965, **53**, pp. 164–165
3 CRANE, H. D.: 'Neuristor—a novel device and system concept', *Proc. IRE*, 1962, **50**, pp. 2048–2060
4 NAGUMO, J., YOSHIZAWA, S., and ARTIMOTO, S.: 'Bistable transmission lines', *IEEE Trans.*, 1965, **CT-12**, pp. 400–412
5 NISHIZAWA, J., and HAYASAKA A.: 'Two-line neuristor with active element in series and in parallel', *Int. J. Electron.*, 1969, **26**, pp. 437–469
7 ROSENGREEN, A.: 'Experimental neuristor gives nerve-like pulse propagation', *Electronics*, 1963, **36**, 9, pp. 25–27
8 SCOT, A. C.: 'Neuristor propagation on a tunnel diode loaded transmission line', *Proc. Inst. Elec. Electron. Eng.*, 1963, **51**, p. 240
9 WILAMOWSKI, B., YOKOGAWA, H., and NISHIZAWA, J.: 'Neuristor propagation in low impedance line', *Int. J. Electron.*, 1970, **29**, pp. 101–137
10 WILAMOWSKI, B.: 'A novel concept of neuristor logic', *Int. J. Electron.*, 1972, **33**, pp. 659–663

ERRATUM

SHARON, T. M., MARADUDIN, A. A., and CUNNINGHAM, S. L.: 'Rectangular-ridge vibrational modes', *Electron. Lett.*, 1974, **10**, pp. 229–230

It has been kindly pointed out by P. E. Lagasse that in Fig. 2 the lowest flexural mode spectra for the infinite plate (Lamb wave) and the finite ridge of $H/W = 3$ are incorrectly drawn, owing to an erroneous interpretation of Fig. 3 of Reference 2. To correct these two mode spectra, *qd* should be multiplied by Ω_R/Ω for the value of Ω/Ω_R corresponding to the particular *qd*. Fig. 2 is shown correctly below.

The agreement between our theoretical results for a semi-infinite ridge and those for the infinite plate (as well as the experimentally determined result for the finite ridge) is better than previously indicated, especially for $qd \gtrsim 1$. However, although closer now to the semi-infinite-ridge mode, the lowest flexural mode for the ridge with a substrate still lies above that for the infinite plate. Therefore our original conclusion concerning the cantilever aspect of finite ridges of this height/width ratio is still valid

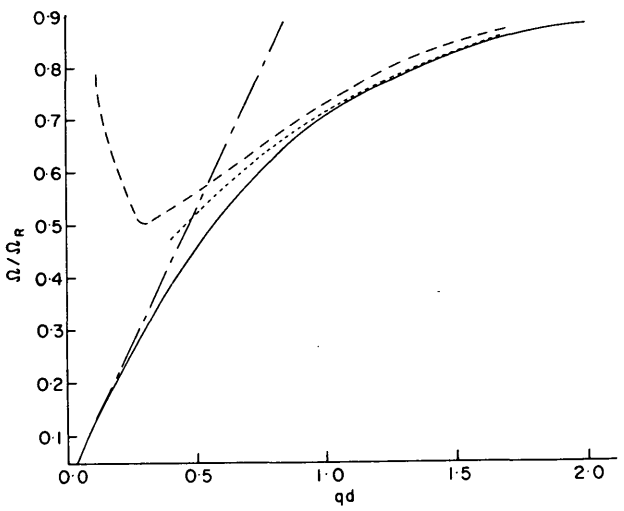

Fig. 2 *Ratio Ω/Ω_R as function of qd for lowest a.s.f. mode of Duralumin 17S ridge*

Broken line is experimental result for height/width ratio of 3;[2] solid line is theoretical result of this work; dotted line is lowest flexural mode of an infinite plate[2] (Lamb wave); broken–dotted line is result from thin-plate theory for flexural wave propagating along the free edge of a semi-infinite ridge[9]